ELLIOTT 900

Volume 4: ENGINEERING MAINTENANCE

Part 1: BASIC EQUIPMENT

Section 3: PAPER TAPE STATION (DPA 211, 221 and 231)

CONTENTS

Page

Page

END-OF-TEXT FIGURES

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INFORMATION BULLETIN No. 1

Amend Section 4.1.3 of the 903 Manual as indicated in this bulletin. The bulletin must then be filed after the Contents List of Section 4.1.3.

Page	Issue	Reference	Amendment
30	2	6.5	Delete both references to X51 in this paragraph. Insert in both their respective places: "XPTS 1".

Chapter 1: INTRODUCTION

1.1 Location of Component Parts

The paper tape equipment comprises one tape reader and one tape punch which are free-standing on top of the computer desk. The power supply unit, with its associated control circuitry, and the logic rack are mounted in the left-hand side of the desk. The operator's controls are located on the punch and reader and on a panel housed along the top front edge of the desk.

The position of the parts of the paper tape station are shown in Figure 1.

1.2 Connections

The cables linking the units within the paper tape station, the mains input from the filter unit and the connection to the interface are shown in Figure 2.

1.3 Logic Boards

The circuits of the L. S. A. elements used on the logic boards are described in Section 1 of this Part of the Manual. The tables in Figure 9 provide details of the types of L. S. A. element on each board and the location of any extra components used.

Chapter 2: POWER DISTRIBUTION

2.1 A.C. Supplies

The distribution of the a.c. supplies is shown in Figure 3.

The mains input on TB1 is taken to the contacts of RLA. This relay is energised by a 24 V signal from the interface which is present when the mains ON button on the control unit is operated. A Local/Remote switch is available to bypass the relay contacts when it is required to apply power to the paper tape station only.

The mains supply to the punch motor is further switched by a silicon controlled rectifier which is energised by a signal from the logic.

The output of the transformer CVT is used to light the lamp in the tape reader.

2.2 D.C. Supplies

The distribution of the d.c. supplies is shown in Figure 4.

The d.c. supplies are provided by two units labelled PSA and PSB. PSA is a type NS-ELL/006, catalogue No. 11224, and provides the +6 V and -6 V supplies at current ratings of 3 A and 1 A respectively. PSB is a type ES1000/28, catalogue No. 11225, and provides the +28 V supply at a current rating of 10 A.

Details of these units can be obtained from the manufacturer's handbooks.

2.3 Over-Voltage Protection

An over-voltage protection circuit is connected across the +6 V and -6 V d.c. outputs to protect the logic boards from damage due to a rise in level of either of these supplies. Under normal operating conditions, the lamps will be lit and no current taken by the circuit.

If either of the d.c. outputs start to rise then current will be drawn through the corresponding zener diode and current applied to the thyristor. Dependent on the ambient temperature and component tolerances, the thyristor will be triggered when the d.c. level has risen to a value between 6.5 V and 10.0 V.

When the thyristor conducts, a short circuit is applied across the output terminals of the power unit, causing the appropriate fuse to blow and the lamp to extinguish.

2.4 Hour Meter

To measure the total time that the computer is switched on, an Hour Meter can be provided as an optional facility. This is located on the rear of the power supply unit as shown in Figure 1.

The meter is connected to TB1 pins 4 and 5, the same pins as feed the a. c. mains supply to the paper tape reader. When the ON button on the Control Unit is pressed, the processor power supplies are up sequenced and a 24V signal is sent to the paper tape station to energise RLA (Figure 3). The contacts of RLA connect the a. c. mains to the Reader and Teleprinter (if fitted) and hence cause the Hour Meter to be energised.

Chapter 3: PAPER TAPE INPUT LOGIC

3.1 Introduction

This chapter contains a functional description of the logic associated with the paper tape reader. The logic is shown in Figures 5 and 6.

It is assumed throughout that the reader is familiar with the appropriate specifications in Volume 1 of this Manual.

3.2 Typical Cycle

Assuming that the reader has been loaded, a brief description of the normal cycle of events is as follows.

On receipt of an input select signal, a timing sequence is initiated which gates the data from a buffer register onto the interface lines and then sends a reply to the central processor.

The data is accepted by the processor and the input select signal removed. This causes the reader clutch solenoid to be energised and the tape advanced. When a sprocket hole is detected, a loading timing sequence is started which resets the buffer register and then gates the data from the new character into the register. The clutch solenoid is de-energised and the tape movement stopped.

The reader stays in this position until another input select signal is received from the central processor.

3.3 Channel Selection

An input from the tape reader is selected according to the position of the Select In switch and/or the type of system in use. For an input to be taken from the reader RIN must be true.

If a teleprinter is not used then its associated logic is omitted, and the T/P LINK on board 22 will not be present. This holds the input to gate 14/2B (i.e. board 14, element 2B) at a true level and means that TIN is always false and RIN always true. The position of the Select In switch has no effect on the logic.

When a teleprinter is used, TIN will be false and RIN true if the Select In switch is set to READER, or AUTO with the interface signal [ADDRESS BIT 3] false. TIN will be true and RIN false if the Select In switch is set to TELEPRINTER, or AUTO with the interface signal [ADDRESS BIT3] true.

3.4 Data Flow

Data from the reader, in the form of an 8-bit character $\langle\overline{R1}\rangle$ to $\langle\overline{R8}\rangle$, is stored in a buffer register 1A/1A etc. on board 7, until demanded by the central processor. The buffer is reset by R/S going true and is immediately loaded due to GATE going true.

When a data transfer is required, the signal RDIN is made true and the content of the buffer gated, at 1A, 2A etc. on board 15, to the interface input lines [IR1] to [IR8]. The data remains on the lines until accepted by the processor, when RDIN will go false.

3.5 Reader Timing

3.5.1 Data Transfer

When a data transfer is required, interface signal [STR] is made true. If the reader has been selected, then RIN is true and TIN false. This means that RWAIT must go false before $\overline{\text{INBUSY}}$ can go true. This occurs at the end of a tape movement when the load bistable 6/5A/5A is set and L2 goes true.

INSEL and $\overline{\text{INBUSY}}$ being true makes the output of 16/1A go false and set the bistable 16/4A/4A to produce $\overline{\text{ACT}}$. A 1 μs delay is introduced before $\overline{\text{ACT1}}$ goes false and triggers the monostable 16/5B/4B to produce 680 ns pulses ACT* and $\overline{\text{ACT*}}$. The 1 μs delay is produced by the capacitor to earth and is to prevent small spikes propagating spurious ACT* and ACT** pulses. Another 680 ns pulse ACT** generated by 16 /7B sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

When $\overline{\text{ACT1}}$ goes false the YES output of 16/7A goes true. INSEL and RIN are also true and hence RDIN goes true and $\overline{\text{RDIN}}$ false. The data is gated onto the interface lines by RDIN.

With ACT* and RDIN both going true the load bistable 6/5A/5A is reset and L2 goes false. RWAIT therefore goes true and $\overline{\text{INBUSY}}$ false to inhibit further $\overline{\text{INSEL}}$ signals until the reader has completed its transfer cycle.

$\overline{\text{RDIN}}$ going false prevents the reader clutch solenoid being energised.

3.5.2 Tape Movement

When the central processor has accepted the data on the interface lines, [STR] goes false. SELECT, therefore, goes false and resets the timing chain bistables 16/4A/4A and 16/2B/2B. INSEL going false and $\overline{\text{ACT1}}$ true cause RDIN to go false and $\overline{\text{RDIN}}$ true. All inputs to the tape drive gate 5/2B are now true and $\overline{\text{CLUTCH}}$ goes false to energise the solenoid.

Tape is advanced until a sprocket hole is detected when $\overline{\text{<SPKT>}}$ goes false and triggers the 30 µs monostable 6/1B/1A. At the same time data signals from the tape should have become false. The 30 µs pulse forms a delay to ensure that in cases of skewing and worst case circuit tolerance this condition is achieved.

At the end of the delay the bistable 6/2A/3A is set and this triggers the monostable 6/2B/2A. The output is R/S, a 330 ns pulse used to reset the buffer register.

The pulse is also gated with $\overline{\text{RDIN}}$ and $\overline{\text{L2}}$, which are both true, to trigger a monostable 6/3B/4A and produce a 600 µs GATE pulse to enter data into the buffer register.

The trailing edge of the GATE pulse produces a 330 ns pulse from 2B to set the load bistable 6/5A/5A. $\overline{\text{L2}}$ going false and L2 true. $\overline{\text{L2}}$ causes $\overline{\text{CLUTCH}}$ to go true and the tape movement is stopped. L2 causes RWAIT to go false and allow the next $\overline{\text{INSEL}}$ signal to be accepted.

3.6 Operator's Controls

3.6.1 Hold-Up Lamp

This is lit each time that a reader input is demanded, both $\overline{\text{INSEL}}$ and TIN being false. The lamp remains lit until data transfer is completed and $\overline{\text{INSEL}}$ goes true.

3.6.2 Read Button

The Read button is operated to load the reader after a new tape has been fitted or to restart after the Stop button has been pressed. Operation of the Read button causes $\overline{\text{LOAD}}$ to go false and this signal is used for three functions.

The bistable 5/2A/3A is set and the output goes true. This causes the Stop lamp to go out and also applies a true signal to gate 5/2A controlling RWAIT.

The pulse generator 5/1B is triggered and LOAD*, a 220 μs pulse, is produced.

$\overline{\text{LOAD}}$ and LOAD* are applied to the bistable 6/7A/6A and as UNLOAD is false due to Tape Out switch being closed, the bistable is set and $\overline{\text{UNLOAD}}$* goes true. This causes the Read lamp to go off and $\overline{\text{UNL}}$ to go true. $\overline{\text{UNLOAD}}$* applied to the tape drive gate 5/2B causes $\overline{\text{CLUTCH}}$ to go false and tape movement to start. Tape is advanced until a sprocket hole is detected and <$\overline{\text{SPKT}}$>goes false. The action is then as previously described in 5.2.

The HOLD signal is set false when $\overline{\text{CLUTCH}}$ is true and this ensures that the bistable 6/7A/6A is not reset when $\overline{\text{LOAD}}$ goes true on releasing the Read button.

3.6.3 Stop Button

This button is operated when it is required to stop tape being read. Operation of the button applies a false signal to reset the bistable 5/2A/3A and cause the Stop lamp to light. The false signal from 5/3A11 is also applied to 5/2A5 so that RWAIT is held true preventing an $\overline{\text{INSEL}}$ signal from being accepted. If a reader input is in progress when the Stop button is pressed, the cycle will be completed.

3.6.4 Run Out Button

The button allows tape to be run through the reader at full speed independently of the central processor. Operation of the button causes $\overline{\text{R/O}}$, the output of 5/4A11, to go false which causes UNLOAD to go true. $\overline{\text{R/O}}$ applied to 5/3B1 causes $\overline{\text{CLUTCH}}$ to go false and tape movement to commence.

UNLOAD going true resets the bistable 6/7A/6A causing $\overline{\text{UNLOAD}}$* and $\overline{\text{UNL}}$ to go false and the Read lamp to light. $\overline{\text{UNL}}$ resets the bistable 6/5A/5A and holds $\overline{\text{L2}}$ true during the run-out period.

Tape movement continues until the Run-Out button is released and $\overline{\text{R/O}}$ goes true. The Read button must be operated to set the bistable 6/7A/6A before reading can restart.

3.7 Error Conditions

3.7.1 Tape-Out Switch

This is a micro-switch located beneath the tape guide plate on the reader. It is operated when the plate is raised for loading or unloading of tape and when the end of the tape passes through the plate.

Release of the switch applies a false signal to 5/4A and causes UNLOAD to go true. This in turn resets the bistable 6/7A/6A causing $\overline{\text{UNLOAD}}$* to go false and the Read lamp to light. $\overline{\text{UNLOAD}}$* prevents $\overline{\text{CLUTCH}}$ going false to move the tape, and RWAIT going false to accept an $\overline{\text{INSEL}}$ signal.

3.7.2 Creep Error

This occurs when the tape does not stop quickly enough and a second SPKT pulse is detected. The 30 μs DELAY pulse is gated with L2, and when both are true, a false signal is obtained from 6/4A13. This signal is mixed with $\overline{\text{UNLOAD}}$* the output of 6/7A13 and resets the bistable 6/7A/6A to prevent further reading of the tape.

3.7.3 Hold

This signal is normally held at a false level by the output of gate 5/2B which has the same sense as $\overline{\text{CLUTCH}}$. When a tape movement is initiated, after a data transfer, the output of 5/2B goes false and the input to the regenerable monostable 5/4B goes true. The monostable has a recovery time of 200 ms and if a sprocket hole is not detected and the tape movement stopped within that period, then HOLD will go true. This causes the bistable 6/7A/6A to reset and the Reader to unload.

This condition can occur if the end of the tape has passed the read head, unpunched tape is passed through the reader, or if the tape is caught and prevented from moving.

Chapter 4: PAPER TAPE OUTPUT LOGIC

4.1 Introduction

This chapter contains a functional description of the logic associated with the paper tape punch. The logic is shown in Figures 5,7 and 8.

It is assumed throughout that the reader is familiar with the appropriate specifications in Volume 1 of this Manual.

4.2 Basic Operation

4.2.1 Typical Cycle

Assuming that the motor is running a brief description of the normal cycle of events is as follows.

On receipt of an output signal, a timing sequence is initiated which gates the data from the interface lines into a buffer and then sends a reply to the central processor.

The punching cycle commences on receipt of a synchronising pulse from the punch mechanism. This causes the data solenoids and, an additional millisecond later, the feed solenoid to be energised. The data holes are punched and the tape advanced to the next character position. The buffer is cleared and the punch is then ready to receive the next output signal.

4.2.2 First and Last Cycle

To avoid excessive wear the punch motor is switched on only when it is required to perform a punching operation.

The motor is switched on by the first data output transfer and a one second delay is introduced to allow the motor to attain full speed before punching commences.

On completion of the last data output transfer a period of 5 seconds is allowed before the motor is switched off.

4.3 Channel Selection

An output to the tape punch is selected according to the position of the Select Out switch and/or the type of system in use. For an output to be sent to the punch POUT must be true.

If a teleprinter is not used then its associated logic is omitted and the T/P LINK on board 22 will not be present. This holds the input to gate 14/4B at a true level and means that TOUT is always false and POUT always true. The position of the Select Out switch has no effect on the logic.

When a teleprinter is used TOUT will be false and POUT true if the Select Out switch is set to PUNCH, or AUTO with the interface signal [ADDRESS BIT3] false. TOUT will be true and POUT false if the Select Out switch is set to TELEPRINTER, or AUTO with the interface signal [ADDRESS BIT3] true.

4.4 Data Flow

Data to the punch in the form of an eight-bit character is present on the interface lines [OP1] to [OP8] when an [STP] signal is sent from the central processor.

At the end of a data output and when the equipment is first switched on, the BUFF R/S signal from 11/6A12 resets the buffer bistable 10/1A/1A etc. such that the outputs 10/1A12 etc. are true.

$\overline{\text{PD OUT}}$ is inverted by 10/4B13 and 10/5B12 and then gated with the data lines $\overline{\text{OUT1}}$ etc., the bistable outputs 10/1A12 etc. being left true if the corresponding data line is false, and being set false if the data line is true. $\overline{\text{PUNCH}}$* is inverted by 10/5B13, gated with the outputs of the above bistables at 10/2B etc., the appropriate punch solenoids being energised.

$\overline{\text{PUNCH}}$* is derived from the monostable 11/2B/4A which is triggered on receipt of a true <SYNC> pulse from the motor mechanism. The false $\overline{\text{FEED}}$ pulse is effectively the same as $\overline{\text{PUNCH}}$* but is delayed by one millisecond. At the end of $\overline{\text{PUNCH}}$* the BUFF R/S pulse is generated by monostable 11/5B/6A to reset the buffer bistables.

4.5 Punch Timing

4.5.1 Data Transfer

When a data transfer is required, interface signal [STP] is made true. If the punch is selected then POUT is true and TOUT false. This means that PWAIT must go false before $\overline{\text{OUTBUSY}}$ can go true. This occurs at the end of a punching operation when the bistable 12/4A/4A is reset and $\overline{\text{L}}$ goes true.

OUTSEL and $\overline{\text{OUTBUSY}}$ being true makes the output of 16/1A go false and set the bistable 16/4A/4A to produce $\overline{\text{ACT}}$. A 1 μs delay is introduced before $\overline{\text{ACT1}}$ goes false and triggers the monostable 16/5B/4B to produce 680 ns pulses ACT* and $\overline{\text{ACT}}$*. The 1 μs delay is produced by the capacitor to earth and is to prevent small spikes propagating spurious

ACT* and ACT** pulses. Another 680 ns pulse ACT** generated by 16/7B sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

When $\overline{\text{ACT1}}$ goes false the YES output of 16/7A goes true. ACT* goes true for 680 ns and as OUTSEL and POUT are also true then $\overline{\text{PDOUT}}$, from 16/6B12, will go false for 680 ns. This pulse gates the data from the interface lines into the buffer bistables 10/1A/1A etc. and also sets the bistable 12/4A/4A causing $\overline{\text{L}}$ to go false and L true.

With $\overline{\text{L}}$ going false PWAIT goes true and $\overline{\text{OUTBUSY}}$ false to inhibit further $\overline{\text{OUTSEL}}$ signals until the punch has completed its punching cycle.

4.5.2 Motor Timing

When $\overline{\text{L}}$ goes false the output of 12/4A13, the OK signal, goes true. The OK signal is used to trigger the 5-second regenerable monostable 12/3B and the 100 ms pulse generator 12/5A/5B.

Assume that no data transfer has taken place for at least 5 seconds then, on the first transfer OK will have been false long enough for the output of regenerable monostable 12/3B to have returned to a false level. Thus SCR will be true, the bistable 12/1B/1B will be reset and MOTOR ON false.

The OK signal going true causes the output of 12/3B to go true and hence SCR will go false switching mains power to the punch motor.

The 100 ms pulse from 12/5B triggers the 1 second regenerable monostable 12/2B. When the monostable recovers the output becomes false and the 50 µs pulse generator 12/4B is triggered. This pulse sets the bistable 12/1B/1B causing MOTOR ON to go true and enable punching to proceed.

The motor remains switched on with SCR false and MOTOR ON true until $\overline{L}$ has been true for at least 5 seconds. If $\overline{L}$ goes false within the 5 second period then the above state will continue for a further 5 seconds. Note also that $\overline{R/O}$ has the same effect as $\overline{L}$.

4.5.3 Punching Signals

A synchronising pulse <SYNC> occurs once per cycle of the motor and from it the punch and feed signals are derived.

When the <SYNC> pulse occurs the monostable 11/1B/2A is triggered and a 40 µs pulse produced. If at the same time, MOTOR ON and OK are true, the output of gate 11/3A goes false to trigger the monostable 11/2B/4A. The output on 11/4A13 is $\overline{\text{PUNCH}}$ which goes false for a period of 5 ms. This causes $\overline{\text{PUNCH}}$* to go false also for 5 ms to energise the solenoids in the punching mechanism. A description of the solenoid driver board is contained in Chapter 5.

The 1 ms monostables 11/4B/3A and 11/3B/2A together with gates 11/4A and 11/5A produce $\overline{\text{FEED}}$ which is identical to $\overline{\text{PUNCH}}$* but delayed by 1 ms. When $\overline{\text{PUNCH}}$ goes false the 1 ms monostable 11/4B/3A is triggered, the false output on 11/3A11 holding $\overline{\text{FEED}}$ true. At the end of the 1 ms period both inputs to gate 11/5A are true and $\overline{\text{FEED}}$ goes false to commence movement of the tape. When $\overline{\text{PUNCH}}$ returns to true the monostable 11/3B/2A is triggered and this maintains the true input to gate 11/5A for 1 ms.

Also when $\overline{\text{PUNCH}}$ returns to a true level, the monostable 11/5B/6A is triggered causing BUFF R/S to go true for 470 ns. This pulse is used to reset the data buffer bistables and the bistable 12/4A/4A causing $\overline{\text{L}}$ to go true. This means PWAIT goes false and the punch is ready to accept the next $\overline{\text{OUTSEL}}$ signal.

4.6 Operator's Controls

4.6.1 Reload Button

This button is operated to override a tape low condition or after a new reel of tape has been fitted into the punch.

Operation of the button applies two false inputs to reset the bistable 12/2A/2A. This causes $\overline{\text{LOW}}$ to go true and the Reload lamp to extinguish. If the button is held down, then a tape low condition can be overridden.

4.6.2 Run-Out Button

This button is operative at all times and causes the punch to continuously output blank tape.

Operation of the button causes $\overline{\text{R/O}}$ to go false and this holds OK and therefore MOTOR ON at a true level. All <SYNC> pulses from the motor mechanism will be accepted and a series of $\overline{\text{FEED}}$ pulses produced.

With the false $\overline{\text{R/O}}$ signal applied to 11/2A, then PWAIT is held true and $\overline{\text{OUTSEL}}$ signals cannot be accepted. Thus $\overline{\text{PDOUT}}$ remains true and the bistable 12/4A/4A remains reset with L false. The L signal applied to 11/6A holds $\overline{\text{PUNCH}}$* at a true level and prevents any data holes from being punched.

4.7 Error Conditions

4.7.1 Tape Low

This is a microswitch which closes when the supply of tape on the spool is nearly exhausted.

Closing of the contacts applies a true signal to set the bistable 12/2A/2A causing $\overline{\text{LOW}}$ to go false and the Reload lamp to light. With $\overline{\text{LOW}}$ held false PWAIT is held true and no $\overline{\text{OUTSEL}}$ signals can be accepted by the punch. If the Reload button is held down, the error condition can be overridden.

4.8 Reset Signals

4.8.1 I.RESET

This is a true pulse which is generated within the paper tape station from 15/6A13 when the equipment is first switched on. The pulse is used to ensure that SCR remains true during this period and the motor is not switched on.

4.8.2 $\overline{\text{RESET}}$

This signal from 15/7A13 is derived from the [RESET] signal generated in the central processor. The signal goes false when the equipment is first switched on and also when the Reset button is operated. The signal remains false until the Jump button is pressed.

$\overline{\text{RESET}}$ going false causes BUFF R/S to go true and reset the data buffer bistables 10/1A/1A etc.

Chapter 5: READER/PUNCH DRIVERS

5.1 Introduction

The Reader/Punch Driver board is a type DPS13 and is located in position 4 of the logic rack. The board contains eleven solenoid driver circuits, nine for the punch, one for the reader and one spare. A common under-voltage protection circuit is also provided for all but the spare driver circuit. The protection circuit prevents operation of the drivers when either the +6 V or +28 V d.c. supplies are low. If one or both of these supplies is low, the drive circuit may not operate correctly and hence cause malfunction of the punch or reader. The layout of the components on the printed circuit board is shown in Figure 10.

5.2 Under-Voltage Protection Circuit

A circuit diagram is shown in Figure 10. When the equipment is first switched on and before the d.c. power rails have reached their operating levels, VT1 is reverse biased and VT2 conducting. As the +28 V rail rises in level current flows through R1, R2, MR2, MR3 and R3 until the junction of R2 and MR2 is at a high enough potential to cause MR1 to perform its zener function. This occurs when the d.c. rail reaches approximately 15 V, the zener voltage is 4.7 V. The d.c. level on the base of VT1 fails to around 3.3 V. Therefore when the +6 V rail rises to approximately 4 V, VT1 will conduct causing VT2 to cut off.

During operation of the equipment if the +6 V level fails to below 4 V then VT1 will be reverse biased and VT2 will conduct. Similarly, if the +28 V level fails sufficiently to prevent MR1 from performing its zener function, the level on the base of VT1 rises causing the transistor to cut off and VT2 to conduct.

5.3 Driver Circuit

A circuit of the driver is shown in Figure 10. There are eleven circuits, ten of which are connected via the diodes MR1 to the under-voltage protection circuit. If the d.c. rails are at a satisfactory working level then a false input signal to the drive circuit causes the level on the base of VT1 to fall and the transistor to conduct. The level on the base of VT2 therefore rises, the transistor oonducts, and the solenoid is energised. A true input to the circuit holds VT1 and VT2 in the off state.

The diode MR4 is to suppress the voltage surge generated during the switch off period.

5.4 Action of Protection Circuit

The collector of VT2 in the protection circuit is connected to the cathode of MR1 in ten of the drive circuits. When either or both of the d.c. supplies are low, VT2 in the protection circuit is conducting. If the input to the drive circuit goes false, diode MR1 in the drive circuit is forward biased and this will prevent VT1 from switching on.

When the d.c. rails have reached a satisfactory level, VT2 is reverse biased. If the input to the drive circuit now goes false, diode MR1 is reverse biased and hence the level on the base of VT1 will fall and cause the drive circuit to energise the solenoid.

Chapter 6: MAINTENANCE AND TEST PROGRAMS

6.1 Introduction

These instructions are intended to supplement and not replace the Maintenance Instructions detailed in the Manufacturer's handbooks, which should still be followed as closely as possible.

The instructions are divided into two categories.

Class I should be carried out at four weekly intervals if the system contains line printers, magnetic tapes or data discs, otherwise it may be carried out every six weeks. These periods are based on an average working day of eight hours. If the equipment is consistently used for longer than eight hours per day, maintenance should be carried out more frequently.

Class II is subject to the same provisions as Class I, but is based on a twelve-weekly period.

6.2 Tape Punch

6.2.1 Introduction

The punch will retain its accuracy and reliability if it is properly maintained. Although it will perforate tape at high and low speeds, the operating life is increased if operated at low speeds.

6.2.2 Class I Maintenance

(1) The punch should be thoroughly cleaned with a lint-free cloth to remove dust and grease

accumulations. A brush may be used to reach inaccessible areas. Care should be taken to avoid damage to delicate parts of the instrument.

(2) Check that all wiring is intact and securely terminated.

(3) Ensure that nuts and screws are tightened, and locked if required.

(4) Inspect the instrument for signs of deterioration or wear which may cause trouble at a later date.

(5) Check the clearance between adjacent moving parts and for any signs of insufficient lubrication.

(6) Check that all data holes and the feed hole are clearly punched. If this check is not satisfactory, the punching block and punching mechanism should be inspected.

(7) Using the paper tape gauge, ensure that the feed holes are correctly related to the guiding edge of the tape, the slot in the gauge lying centrally over the holes.

(8) Rotate the flywheel and check that the feed pawl is not under or overthrowing the feed wheel.

(9) Check that the tape reel brake is operating satisfactorily.

(10) Lubricate all parts as detailed in the manufacturer's handbook.

6.2.3 Class II Maintenance

(1) Carry out Class I Maintenance.

(2) Check that the tape low contacts close when approximately 0.5 inch thickness of tape remains on the spool. Adjust as necessary.

(3) Check that all armatures are attracted to the pole pieces when their solenoids are energised. With the armature in the attracted position, check that the gap between the armature and the pole piece is within the limits .003 to .001 inch at the point of least clearance.

(4) Ensure that the clearance between the blocking pawls and the long toggle arms is within the limits .003 to .002 inch.

6.3 Tape Reader

6.3.1 Introduction

The reader is an electro-mechanical device designed to provide high speed input for computer processors. The maximum rated speed is 250 characters per second.

The device is highly reliable and accurate, and can be made to retain these qualities if properly maintained.

6.3.2 Class I Maintenance

(1) Clean the outside of the reader.

(2) Clean the bulb, prism and window with an anti-static cloth. Replace the bulb if the filament is broken or the glass envelope is discoloured. Check the prism for scratches or crazing.

(3) Check that the tape guides have not been scored by the tapes.

(4) Using a small stiff brush remove any dust, etc. from the brake assembly.

(5) Using gauge D4/22/A206 ensure that the two adjustable tape guide posts can be correctly positioned for all widths of tape.

(6) Check that the light pattern thrown on the holes under the prism is of the correct size and shape. There should be a lighted area which is wider than the holes and has roughly parallel sides evenly disposed about the holes.

(7) Check that the gap between the pinch roller and capstan is 0.0065 to 0.007 inch.

(8) Check that the brake pad is 0.002 to 0.004 inch above the top plate.

(9) Check that the clutch pressure is 320 to 360 gm. Check that the standing brake pressure is within the limits 45 to 55 gm.

(10) Check that all nuts and screws are tight.

(11) Lubricate threads of Plessey plugs with a light grease.

(12) Lubricate all parts as detailed in the manufacturer's handbook.

(13) Check the waveform of the sprocket and data hole outputs. Details are contained in the manufacturer's handbook.

(14) Inspect the hand spooler and ensure the rim is smooth.

6.3.3 Class II Maintenance

(1) Carry out Class I Maintenance.

(2) Check that the pinch rollers and capstan are parallel within 0.0005 inch and that the end float on the pinch roller is between 0.006 and 0.009 inch. Check that the roller is not worn and rotates freely.

(3) Inspect the upper and lower brake pads for wear. Any sign of grooving by the tape should be removed by machining or stoning flat or by replacement of the pads.

(4) Check, using an Avometer, that the lamp voltage is 9.2 V $\pm$ 0.5 V.

(5) With no tape in the reader, energise the clutch and check that the gap between the pinch roller and capstan is 0.001 to 0.002 inch.

(6) Check the power unit outputs. They should be within:-

5.5 V to 6.5 V (two supplies)

and 23.8 V to 32.2 V

all for a mains input of selected voltage $\pm$ 10%.

6.4 Setting-Up a Punch

6.4.1 Punching a Full-House Tape

(1) Ensure that the MODE switch is set to TEST.

(2) Set the eight least significant keys of the word generator to the '1' position.

(3) Set the ENTER key to the up position and return to centre position.

(4) Set the word generator keys to 15 6144.

(5) Operation of the OBEY key will cause the punch to produce a full-house tape. The key has three positions, the centre one being normal or off. In the up position, a full-house is punched for each operation of the key and in the down position the punch continuously produces full-house tape.

6.4.2 Spring Adjustments

(1) Set the equipment to produce a full-house tape from the punch as described in paragraph 6.4.1.

(2) Loosen the armature restoring spring locknuts on the code 1 magnet. Tighten the spring carefully until the oode 1 hole is just not punched. Tighten the locknuts and ensure that the code hole is still not punched. If on tightening the spring, maximum tension is reached and the code hole is still punching, tighten the locknuts for maximum tension and omit the adjustment in sub-paragraph(5).

(3) Repeat sub-paragraph (2) for the other seven code magnets.

(4) Loosen the locknuts on the feed magnet armature restoring spring. Tighten the spring to maximum tension. If tape is not being fed through the punch, slacken the spring carefully until tape is just being fed. Give the spring adjusting nut one complete turn in the direction to slacken the spring, then tighten the locknuts.

(5) Loosen the locknuts on the armature restoring spring of the code 1 magnet. Slacken the spring carefully until code hole 1 is just punched. Check that the hole is also punched under stop/start conditions. Tighten the locknuts.

(6) Repeat sub-paragraph (5) for the other seven code magnets, ensuring that a full-house is being punched.

(7) Slacken the locknuts on the armature restoring spring of the code 1 magnet. Give the spring adjusting nut one complete turn in the direction to slacken the spring, then tighten the locknuts.

(8) Repeat sub-paragraph (7) for the other seven code magnets.

(9) On completion of these adjustments, the punch mechanism should be lubricated as detailed in the manufacturer's handbook.

6.5 Test Program

A diagnostic program is not provided for the paper tape station. On completion of Class I or Class II maintenance, the operator's daily test program ~~X51~~ XPTS 1 should be run to ensure the correct functioning of the equipment. Satisfactory working for approximately half a reel of tape, ensures that the equipment is in a working state. ~~X51~~ XPTS 1 is described in Section 3.1.2.